

What is claimed is:

1 1. A circuit comprising:
2 a differential pair to receive a differential signal at a bulk input port and to
3 generate an output signal at an output port.

1 2. The circuit of claim 1 further including a common gate of the differential
2 pair to receive a gate bias voltage.

1 3. The circuit of claim 1 further including a common source/drain terminal of
2 the differential pair coupled to a current source.

1 4. The circuit of claim 1 further including an amplifier coupled to the output
2 port.

1 5. The circuit of claim 1 wherein the output signal is a function of the
2 differential signal.

1 6. The circuit of claim 1 further including an active load coupled to the drain
2 output port.

1 7. The circuit of claim 6 wherein the active load includes a transistor having a
2 drain terminal shunted to a gate terminal.

1 8. The circuit of claim 6 wherein the active load includes a transistor.

1 9. The circuit of claim 6 wherein the active load includes a transistor having a
2 bulk terminal coupled to a reference node.

1 10. The circuit of claim 6 wherein the active load includes a transistor pair
2 having a common gate.

- 1 11. A circuit comprising:
 - 2 a first transistor having a first bulk and a first drain;
 - 3 a first input node at the first bulk; and
 - 4 a first output node at the first drain.
- 1 12. The circuit of claim 11 further including a first gate of the first transistor to
2 receive a bias voltage.
- 1 13. The circuit of claim 11 wherein the first transistor includes a first source to
2 receive a bias current.
- 1 14. The circuit of claim 11 wherein the first transistor includes a first source
2 coupled to a supply voltage.
- 1 15. The circuit of claim 11 further including a resistive load coupled to the first
2 output node.
- 1 16. The circuit of claim 11 further including a second transistor having a second
2 gate in common with the first gate, the second transistor having a second bulk and a
3 second drain;
 - 4 a second input node at the second bulk; and
 - 5 a second output node at the second drain.
- 1 17. The circuit of claim 16 wherein the first transistor and the second transistor
2 include a common source.
- 1 18. The circuit of claim 17 further including a current source coupled to the
2 common source/drain.

1 19. A method comprising:
2 biasing a gate terminal of a first transistor in an amplifier;
3 providing an input signal to a bulk terminal of the first transistor; and
4 generating a first output signal as a function of the input signal at a first
5 output terminal coupled to a first drain terminal of the amplifier.

1 20. The method of claim 19 wherein biasing includes providing a bias current.

1 21. The method of claim 19 wherein providing the input signal includes
2 providing a first differential input signal to the first transistor of a differential pair
3 and providing a second differential input signal to a second transistor of the
4 differential pair.

1 22. The method of claim 21 further including generating a second output signal
2 at a second output port coupled to a second drain terminal of the differential pair,
3 the second output signal generated as a function of the first differential input signal
4 and the second differential input signal.

1 23. The method of claim 21 further including biasing a source terminal of the
2 first transistor.

1 24. The method of claim 23 wherein biasing the source terminal includes
2 providing a current source.

1 25. The method of claim 21 wherein the first transistor is in a saturation mode.

1 26. A communication device comprising:
2 an antenna having an antenna output;
3 a first amplifier including a transistor having a bulk terminal coupled to the
4 antenna output and a bias node coupled to a gate terminal of the transistor; and

5 a second amplifier having an input coupled to a first drain node of the first
6 amplifier.

1 27. The device of claim 26 wherein the bulk terminal is coupled to the antenna
2 output via a tuner.

1 28. The device of claim 26 further including a second source terminal of the
2 transistor coupled to a power supply.

1 29. The device of claim 28 wherein the power supply includes a current source.

1 30. The device of claim 26 wherein the gate terminal is coupled to a voltage
2 supply.

1 31. The device of claim 26 further including a resistor coupled to the first drain
2 node and a reference node.

1 32. The device of claim 26 wherein the first amplifier includes a differential
2 amplifier.

1 33. A system comprising:
2 a driver having a pair of differential output terminals;
3 a receiver having a pair of differential input terminals coupled to the pair of
4 differential output terminals wherein each input terminal is coupled to a bulk
5 terminal of a transistor.

1 34. The system of claim 33 wherein a gate terminal of each transistor is biased.

1 35. The system of claim 33 wherein the receiver includes an output terminal
2 coupled to a drain terminal of the transistor.

1 36. The system of claim 33 wherein the transistor is biased in a saturation
2 region.